What is claimed is:

1. A transistor of a semiconductor device, comprising:

an epitaxial channel region disposed on an active region of a semiconductor substrate;

a stacked structure of an insulating film and an epitaxial source/drain junction layer disposed at both sides of the channel region; and

a stacked structure of a gate insulating film and a gate electrode disposed on the epitaxial channel region, wherein at least a portion of the gate insulating film overlap with the source/drain junction layer.

2. The transistor of claim 1, wherein the insulating film is an oxide film or a nitride film.

3. The transistor of claim 1, wherein the insulating film and the source/drain junction layer have a thickness ranging from 50 to 1000Å, respectively.

4. The transistor of claim 1, further comprising a device isolation film defining the active region, the thickness of the device isolation film being substantially the same as that of the stacked structure of the insulating film and the source/drain junction layer.

5. The transistor of claim 1, wherein the source/drain junction layer and the channel region consist of epitaxial Si layers.

6. The transistor of claim 1, wherein the thickness of the epitaxial channel region is substantially the same as that of the stacked structure of the insulating film and the source/drain junction layer.

7. A method for forming a transistor of a semiconductor device, comprising the steps of:

forming a stacked structure of a first epitaxial layer and a second epitaxial layer on a semiconductor substrate;

forming a device isolation film of trench type defining an active region, wherein a thickness of the device isolation film is substantially the same as that of the stacked structure;

implanting an impurity into the second epitaxial layer using the device isolation film as a mask;

sequentially forming a thermal oxide film and a sacrificial film on the entire surface of the resulting structure;

etching the sacrificial film, the thermal oxide film, and the second and first epitaxial layers using a gate

electrode mask to form an opening exposing the semiconductor substrate;

removing the first epitaxial layer to form an under-cut under the second epitaxial layer;

forming an insulating film filling the under-cut;

growing a third epitaxial layer on the semiconductor substrate exposed by the opening;

removing the sacrificial film and the thermal oxide film;

implanting an impurity into the third epitaxial layer to form a channel region; and

forming a gate electrode on the channel region.

8. The method of claim 7, wherein the first epitaxial layer is an epitaxial SiGe layer having a thickness ranging from 50 to 1000Å which is grown under an atmosphere of a mixture gas of (i) a gas selected from the group consisting of GeH_4, SiH_4, SiH_2Cl_2 and combinations thereof, (ii) HCl and (iii) H_2.

9. The method of claim 7, wherein the second epitaxial layer and the third epitaxial layer are epitaxial Si layers having a thickness ranging from 50 to 1000Å and 100 to 2000Å, respectively, each of which is grown under an atmosphere of a mixture gas of (i) a gas selected from the group

consisting of SiH_4, SiH_2Cl_2 and combinations thereof, (ii) HCl and (iii) H_2.

10. The method of claim 7, wherein the step of implanting an impurity into the second epitaxial layer is performed using As having a concentration ranging from 1.0E12 to 5.0E13 atoms/cm^2 with an energy ranging from 10 to 100KeV.

11. The method of claim 7, wherein the thickness of the thermal oxide film ranges from 10 to 200Å.

12. The method of claim 7, wherein the sacrificial film is an oxide film, a nitride film or a polysilicon film.

13. The method of claim 7, wherein the step of removing the first epitaxial layer is performed by a wet etching process using a solution containing H_2O, H_2O_2 and NH_4OH at a temperature ranging from 70 to 80°C.

14. The method of claim 7, wherein the step of removing the first epitaxial layer is performed by an isotropic plasma dry etching process using a mixture gas of HBr, O_2 and Cl_2.

15. The method of claim 14, wherein the isotropic plasma dry etching process is performed using microwaves or SF_6 added to the mixture gas.

16. The method of claim 7, wherein the insulating film is an oxide film or a nitride film.

17. The method of claim 16, wherein the oxide film is formed by a chemical vapor deposition which is performed under a pressure of 50Torr at a temperature ranging from 50 to 800°C using SiH_4 and N_2O as source gases.

18. The method of claim 16, wherein the oxide film is formed by a dry or a wet thermal oxidation process at a temperature ranging from 700 to 1100°C.

19. The method of claim 7, wherein the insulating film is formed by an atomic layer deposition.

20. A method for forming a transistor of a semiconductor device, comprising the steps of:

forming a stacked structure of a first epitaxial layer and a second epitaxial layer on a semiconductor substrate;

forming a device isolation film of trench type defining an active region;

forming a dummy gate electrode on the second epitaxial layer;

implanting an impurity into the second epitaxial layer using the dummy gate electrode as a mask;

forming an insulating film spacer at a sidewall of the dummy gate;

forming a thermal oxide film on the entire surface of the resulting structure;

forming a planarized interlayer insulating film exposing the top surface of the dummy gate;

etching the dummy gate and the second and first epitaxial layers therebelow to form an opening exposing the semiconductor substrate;

removing the first epitaxial layer to form an under-cut under the second epitaxial layer;

forming an insulating film filling the under-cut;

growing a third epitaxial layer having an impurity implanted therein on the semiconductor substrate exposed by the opening; and

forming a stacked structure of a gate oxide film and a gate electrode on the third epitaxial layer.

21. The method of claim 20, wherein the first epitaxial layer is an epitaxial SiGe layer having a thickness ranging from 50 to 1000Å which is grown under an

atmosphere of a mixture gas of (i) a gas from the group consisting of GeH_4, SiH_4, SiH_2Cl_2 and combinations thereof, (ii) HCl and (iii) H_2.

22. The method of claim 20, wherein the second epitaxial layer and the third epitaxial layer are epitaxial Si layers having a thickness ranging from 50 to 1000Å and 100 to 2000Å, respectively, each of which is grown under an atmosphere of a mixture gas of (i) a gas from the group consisting of SiH_4, SiH_2Cl_2 and combinations thereof, (ii) HCl and (iii) H_2.

23. The method of claim 20, wherein the impurity implanted into the second epitaxial layer is As having a concentration ranging from 1.0E12 to 5.0E13atoms/cm^2 and the implanting step is performed with an energy ranging from 10 to 100KeV.

24. The method of claim 20, wherein a thickness of the dummy gate ranges from 500 to 3000Å.

25. The method of claim 20, wherein the step of removing the first epitaxial layer is performed in a wet etching process or an isotropic dry etching process.

26. The method of claim 20, wherein the insulating film is an oxide film or a nitride film formed by a thermal oxidation, chemical vapor deposition or atomic layer deposition.